This listing of claims will replace all prior versions, and listings, of claims in the application:

In the claims

Claim 1 (original): A programmable logic device comprising:

at least one RAM block generating at least a first multi-bit calculation result;

a shift operation driven by a second multi-bit calculation result and that shifts the second multi-bit calculation result by at least one bit to generate a shifted second multi-bit calculation result; and

a multi-bit adder coupled to the at least one RAM block and which adds the shifted second multi-bit calculation result to the first multi-bit calculation result.

Claim 2 (original): The programmable logic device of claim 1 wherein the at least one RAM block is configured with at least one look up table ("LUT") for generating at least the first multi-bit calculation result.

Claim 3 (original): The programmable logic device of claim 2 wherein the at least one LUT includes a first LUT for generating the first multi-bit calculation result and a second LUT for generating the second multi-bit calculation result.

Claim 4 (original): The programmable logic device of claim 3 wherein the at least one RAM block includes:

a first input address port for inputting at least a first multi-bit word and the first LUT is configured to generate the first multi-bit calculation result the first multi-bit calculation result representing a multiplication of the first multi-bit word with at least a first predetermined coefficient; and

a second input address port for inputting at least a second multi-bit word and the second LUT is configured to generate the second multi-bit calculation result, the second multi-bit calculation result representing a multiplication of the first multi-bit word with at least a second predetermined coefficient.

Claim 5 (original): The programmable logic device of claim 4 wherein the second predetermined coefficient is equal to the first predetermined coefficient.

Claim 6 (original): The programmable logic device of claim 5 wherein the first multi-bit word is input into the first input address port substantially simultaneously with the second multi-bit word being input into the second input address port.

Claim 7 (original): The programmable logic device of claim 6 wherein the first multi-bit word is a first portion of a larger multi-bit word and the second multi-bit word is a second portion of the larger multi-bit word.

Claim 8 (original): The programmable logic device of claim 7 wherein the at least one RAM block includes a first RAM block and a second RAM block, the first RAM block being configured with the first LUT and the second RAM block being configured with the second LUT.

Claim 9 (original): The programmable logic device of claim 7 wherein the first LUT and the second LUT are both included in a single RAM block having the first input address port and the second input address port.

Claim 10 (original): The programmable logic device of claim 6 wherein the number of bits the shift operator shifts the second multi-bit calculation result is equal to the number of bits in the first multi-bit word.

Claim 11 (original): The programmable logic device of claim 2 wherein the at least one RAM block includes an address port for inputting at least a first multi-bit word and a second multi-

bit word and the at least one LUT includes a single LUT configured to generate at least the first multi-bit calculation result and a preliminary second multi-bit calculation result.

Claim 12 (original): The programmable logic device of claim 11 wherein the first multi-bit calculation result represents a multiplication of the first multi-bit word with a predetermined coefficient and the preliminary second multi-bit calculation result represents a multiplication of the second multi-bit word with the predetermined coefficient.

Claim 13 (original): The programmable logic device of claim 12 wherein at least the preliminary second multi-bit calculation result is fed into the multi-bit adder to generate the second multi-bit calculation result.

Claim 14 (original): The programmable logic device of claim 13 further including at least one shift register that shifts based on a clock cycle and which inputs the first multi-bit word into the address port on a first clock cycle and inputs the second multi-bit word into the address port on a second clock cycle.

Claim 15 (original): The programmable logic device of claim 14 wherein the first multi-bit word is a first portion of a larger multi-bit word and the second multi-bit word is a second portion of the larger multi-bit word.

Claim 16 (original): The programmable logic device of claim 15 wherein an output of the multi-bit adder drives the shift operator and the output of the shift operation is fed back into the multi-bit adder.

Claim 17 (original): The programmable logic device of claim 16 wherein the first multi-bit calculation result represents a multiplication of the first multi-bit word with a predetermined coefficient.

Claim 18 (original): The programmable logic device of claim 16 wherein the first multi-bit calculation result represents a multiplication of a first portion of the first multi-bit word with a first

coefficient summed with a multiplication of a second portion of the first multi-bit word with a second coefficient.

Claim 19 (original): The programmable logic device of claim 18 wherein the input to the address port of the at least one RAM block includes a multi-bit bus driven by two smaller busses, each of the smaller busses including at least one shift register.

Claim 20 (original): The programmable logic device of claim 1 wherein the shift operation and multi-bit adder are programmed programmable logic circuitry.

Claim 21 (currently amended): A programmable logic device comprising:

at least one RAM block configured with at least one LUT for generating at least a first multi-bit multiplication result;

a shift operation driven by a second multi-bit multiplication result and that shifts the second multi-bit multiplication result by at least one bit to generate a shifted second multi-bit multiplication result; and

an adder having a first input and a second input wherein the first input is driven by the first multi-bit multiplication result and the second input is driven by the shifted second multi-bit multiplication result, the adder adding the first multi-bit multiplication result to the second shifted multi-bit multiplication result.

Claim 22 (original): The programmable logic device of claim 21 wherein the at least one RAM block includes at least a first LUT and a second LUT, the first LUT for generating the first multi-bit multiplication result and the second LUT for generating the second multi-bit multiplication result.

Claim 23 (original): The programmable logic device of claim 22 wherein the at least on RAM block includes a first RAM block coupled to the adder and a second RAM block coupled to the shift operation.

Claim 24 (original): The programmable logic device of claim 21 wherein an output of the adder drives the shift operation and the output of the shift operation is fed back into the multi-bit adder.

Claim 25 (currently amended): A method of carrying out a multi-bit calculation including:

inputting at least a first multi-bit word into ~~the~~ at least one RAM block configured with at least one LUT;

generating at least a first multi-bit calculation result from the at least one LUT in the at least one RAM block;

generating at least a second multi-bit calculation result;

shifting the at least second multi-bit calculation result by at least one bit to generate a shifted second multi-bit calculation result; and

adding the shifted second multi-bit calculation result to the first multi-bit calculation result.

Claim 26 (original): The method of claim 25 further including:

inputting a second multi-bit word into the at least one RAM block;

wherein configuring at least one LUT includes configuring a first LUT and a second LUT in the at least one RAM block;

generating at least a first multi-bit calculation result includes generating the first multi-bit calculation result from the first LUT; and

generating at least a second multi-bit calculation result includes generating the second multi-bit calculation result from the second LUT.

Claim 27 (original): The method of claim 26 wherein:

generating at least a first multi-bit calculation result includes generating the first multi-bit calculation result representing a multiplication of the first multi-bit word with at least a first predetermined coefficient; and

generating at least a second multi-bit calculation result includes generating the second multi-bit calculation result representing a multiplication of the second multi-bit word with at least a second predetermined coefficient.

Claim 28 (original): The method of claim 27 wherein the second predetermined coefficient is equal to the first predetermined coefficient.

Claim 29 (original): The method of claim 28 wherein:

inputting the first multi-bit word into the at least one RAM block includes inputting the first multi-bit word into a first input address port in the at least one RAM block substantially simultaneously with inputting the second multi-bit word into a second input address port in the at least one RAM block.

Claim 30 (original): The method of claim 29 wherein the first multi-bit word is a first portion of a larger multi-bit word and the second multi-bit word is a second portion of the larger multi-bit word.

Claim 31 (original): The method of claim 30 wherein:

the at least one RAM block includes a first RAM block and a second RAM block; and

configuring at least one LUT includes configuring the first LUT in the first RAM block and configuring the second LUT is the second RAM block.

Claim 32 (original): The method of claim 30 wherein configuring at least one LUT includes configuring the first LUT and the second LUT in a single RAM block having the first input address port and the second input address port.

Claim 33 (original): The method of claim 25 further including inputting a second multi-bit word into the at least one RAM block and wherein:

configuring at least one LUT includes configuring a first LUT in the at least one RAM block to generate at least the first multi-bit calculation result from the first multi-bit word and a preliminary second multi-bit calculation result from the second multi-bit word; and

generating at least a second multi-bit calculation result includes generating the second multi-bit calculation result from an adder which adds shifted second multi-bit calculation result to the first multi-bit calculation result.

Claim 34 (original): The method of claim 33 wherein:

generating the first multi-bit calculation result includes generating a result that represents multiplying the first multi-bit word with a predetermined coefficient; and

generating the preliminary second multi-bit calculation result includes generating a result that represents multiplying the second multi-bit word with the predetermined coefficient.

Claim 35 (original): The method of claim 34 further including:

shifting the first multi-bit word into an address port in the at least one RAM block on a first clock cycle; and

shifting the second multi-bit word into the address port in the at least one RAM block on a second clock cycle.

Claim 36 (original): The method of claim 35 wherein the first multi-bit word is a first portion of a larger multi-bit word and the second multi-bit word is a second portion of the larger multi-bit word.

Claim 37 (original): The method of claim 33 wherein:

generating the first multi-bit calculation result includes generating a result that represents a multiplication of a first portion of the first multi-bit word with a first coefficient summed with a multiplication of a second portion of the first multi-bit word with a second coefficient.

Claim 38 (original): The method of claim 37 including driving the address port of the at least one RAM block with a bus that is driven by two smaller busses, each of the smaller busses including at least one shift register.

Claim 39 (original): The method of claim 25 wherein the multi-bit calculation is carried out in a programmable logic device.